REMARKS

Claims 1-4 and 6 were examined and reported in the Office Action. Claims 1-4 and 6 are rejected. Claims 1, 3, 4 and 6 are amended. Claims 1-4 and 6 remain. Applicant requests reconsideration of the application in view of the following remarks.

I. Claim Objections

It is asserted in the Office Action that claims 1 and 3 are objected to for informalities. Applicant has amended claims 1 and 3 to overcome the informal objections.

Accordingly, withdrawal of the informal objections of claims 1 and 3are respectfully requested.

II. Claim Rejections - 35 U.S.C. §112

It is asserted in the Office Action that claims 1-4 and 6 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claims 1, 3, 4 and 6 to overcome the 35 U.S.C. §112, second paragraph rejections.

Accordingly, withdrawal of the rejection of claims 1-4 and 6 under 35 U.S.C. §112, second paragraph, are respectfully requested.

III. 35 U.S.C. §103(a)

A. It is asserted in the Office Action that claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over Jarboe, Jr. et al (US PG Publication 2004/0153793) in further view of U. S. Patent No. 5,584,003 issued to Yamaguchi et al. ("Yamaguchi"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic criteria

> must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." "*All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 4 contains the limitations of

> [a] method for controlling a tag block, comprising: initializing the tag block in a semiconductor memory device; and performing a data access operation of the semiconductor memory device in response to a physical unit cell address outputted from the tag block sensing a logical cell block address, wherein the initializing the tag block in a semiconductor memory device including: nullifying N+1 number of unit tag tables of the tag block; selecting all of the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables.

Jarboe discloses a method and device that enables testing of multiple embedded memory arrays associated with processor cores on a single chip. Jarboe, however, does not teach, disclose or suggest a tag block having N+1number of unit tag tables for sensing a logical cell block address included in an inputted row address to output a physical unit cell address. The logical cell block address is corresponding to N number of unit cell blocks (i.e., a specification of a semiconductor memory device receiving the inputted row address, and the physical unit cell address is corresponding to N+1 number of unit cell blocks substantially included in the

semiconductor memory device for high speed data access). Further, Jarboe does not teach, disclose or suggest how to enable or initialize the tag block.

Therefore, Jarboe does not teach, disclose or suggest Applicant's amended claim 4 limitations of

> [a] method for controlling a tag block, comprising: initializing the tag block in a semiconductor memory device; and performing a data access operation of the semiconductor memory device in response to a physical unit cell address outputted from the tag block sensing a logical cell block address, wherein the initializing the tag block in a semiconductor memory device including: nullifying N+1 number of unit tag tables of the tag block; selecting all of the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables.

Yamaguchi discloses a control system for controlling a cache tag memory. Yamaguchi, however, does not teach, disclose or suggest a tag block having N+1number of unit tag tables for sensing a logical cell block address included in an inputted row address to output a physical unit cell address. The logical cell block address is corresponding to N number of unit cell blocks (i.e., a specification of a semiconductor memory device receiving the inputted row address, and the physical unit cell address is corresponding to N+1 number of unit cell blocks substantially included in the semiconductor memory device for high speed data access). Further, Yamaguchi does not teach, disclose or suggest how to enable or initialize the tag block.

Therefore, even if Jarboe were combined with Yamaguchi, the resulting invention would still not include all of Applicant's claim 4 limitations. Since neither Jarboe, Yamaguchi, and therefore, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claim 4, as listed above, Applicant's amended claim 4 is not obvious over Jarboe in view of Yamaguchi since a *prima facie* case of obviousness has not been met under MPEP §2142.

Accordingly, withdrawal of the rejection of claim 4 under 35 U.S.C. §103(a) is respectfully requested.

B. It is asserted in the Office Action that claim 6 is rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent 6,557,080 issued to Burger et al ("Burger") in further view of Yamaguchi. Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant's amended claim 6 contains the limitations of

> [a] method for a refresh operation of a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a tag block having N+1 number of unit tag tables for sensing a logical cell block address to output a physical unit cell address, each having M number of registers for sensing an update of data, comprising: nullifying the N+1 number of unit tag tables; selecting all the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables, wherein the N number of unit cell blocks are corresponded to an address and one unit cell block is added for accessing data with high speed.

Yamaguchi discloses a control system for controlling a cache tag memory. Yamaguchi, does not teach, disclose or suggest

> a tag block having N+1 number of unit tag tables for sensing a logical cell block address to output a physical unit cell address, each having M number of registers for sensing an update of data, comprising: nullifying the N+1 number of unit tag tables; selecting all the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables, wherein the N number of unit cell blocks are corresponded to an address and one unit cell block is added for accessing data with high speed.

Burger discloses a cache structure that allows dynamic control of the size and configuration of the data block fetched by the cache from memory. Burger, however, does not teach disclose or suggest

> a tag block having N+1 number of unit tag tables for sensing a logical cell block address to output a physical unit cell address, each having M number of registers for sensing an update of data,

> comprising: nullifying the N+1 number of unit tag tables; selecting all the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables, wherein the N number of unit cell blocks are corresponded to an address and one unit cell block is added for accessing data with high speed.

Therefore, even if Yamaguchi were combined with Burger, the resulting invention would still not include all of Applicant's claim 6 limitations. Since neither Yamaguchi, Burger, and therefore, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claim 6, as listed above, Applicant's amended claim 6 is not obvious over Yamaguchi in view of Burger since a *prima facie* case of obviousness has not been met under MPEP §2142.

Accordingly, withdrawal of the rejection of claim 6 under 35 U.S.C. §103(a) is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-4 and 6, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: October 13, 2006

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on October 13, 2006.

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Jean Svoboda